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Reg. No. : ....

Name : ....

Sixth Semester B.Tech. Degree Examination, June 2015
(2008 Scheme)
08.602 : VLSI DESIGN (TA)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. What are the different processes involved in silicon wafer preparation ?
2. State Flick's theory of diffusion.
3. Explain the principle of electron-beam lithography.
4. Compare the features of CMOS and bipolar technologies.
5. Define threshold voltage for a MOS transistor. What are the parameters on which it depends on ?
6. PMOS is a perfect switch for transmission of logic 1 while NMOS is perfect for transmission of logic O. Justify the statement.
7. Write down the basic principle of dynamic CMOS logic with circuit diagram.
8. Show the critical path in a linear carry select adder scheme and give the expression for critical path delay involved.
9. Draw and explain multiplexer based positive edge-triggered register using master-slave configuration.
10. What are the functionalities of sense amplifiers in memory circuits ?

PART – B

Answer **any two** questions from **each** Module. **Each** question carries **10** marks.

Module – I

11. What is meant by electron stopping and range distribution in ion implantation ? With neat diagram explain the operation of an ion implantation system.

12. With neat sketches explain the fabrication steps involved in p-well CMOS process. What is latch-up problem in CMOS circuits ?

13. a) Explain Czochralski technique of crystal growth. 6

b) Write down the difference between epitaxy and diffusion. 4

Module – II

14. a) Derive the current equation for enhancement mode NMOS transistor in different regions of operations. 6

b) What do you mean by short channel effect of MOSFET ? 4

15. a) Draw the transfer characteristics of CMOS inverter and explain the five regions of operations. 6

b) Obtain the scaling factors for any 4 MOS device parameters in generalized scaling. 4

16. a) Draw the circuit diagram and stick diagram for implementing the logic function $F = \overline{A \cdot (B + C)}$ in static p-well CMOS logic. 6

b) Draw the implementation of a 4 :1 multiplexer using transmission gates. 4

Module – III

17. a) What are the advantages and disadvantages of dynamic latches and registers over static implementations ? 4

b) Draw the structure of a dynamic transmission gate edge-triggered register. What are the clock overlap period constraints to avoid race conditions ? 6

18. a) Explain the operation of a N $\times$ M bit array multiplier. 5

b) Explain the partial product accumulation in a Wallace tree multiplier. 5

19. a) What is meant by controllability and testability with reference to testable designs ? 3

b) What is Built-in self Test (BIST) ? Explain the components in a BIST module with necessary circuits. 7

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